EE/CprE/SE 492 BIWEEKLY REPORT 4

Date: ***October 12th, 2023 – October 25th***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Biweekly Summary

Over the course of the past two weeks, quite a bit of significant work has been completed. After figuring out that some of our assumptions about the harness were wrong, we updated our schematic. With this updated schematic, we had many new components that needed to be created. Most of these new devices have been fully pushed through the analog design flow, including a transmission gate, 2-1 MUX, and 4-1 MUX. The resistor voltage dividers have also been created and are through most of the analog design flow as well.

We also have successfully figured out the Efabless precheck system, which was a big question of ours. We were able to hook up an inverter into the harness in the schematic and then create a layout that matched that. We then pushed that layout through the precheck, and after a bit of playing around with some files and the layout, we were able to successfully pass the precheck with our inverter.

We also began work on creating the layouts for our crossbars, starting with a simple 1T1R design. We were able to complete a layout for the device, and it passed DRC and LVS checks, however, there were property errors in the layout. After asking about this in Slack, the people who maintain the Open PDKs noticed that there were some errors in the ReRAM symbol. This is currently being investigated and should hopefully be resolved within the next week.

We also found out that doing simulations with the ReRAM - in the way that we imagined - is most likely not able to be done. The ReRAM model has flaws, and as such, it has convergency issues when simulating, leading us to not be able to do the simulations using Ngspice. This was brought up to our advisor, who shared the model with someone doing research under him, and he was able to get it to simulate correctly using Cadence. Cadence is much more robust than the simulators we are using, and it can handle the more complicated model. However, this may not be able to help us at this point in our project. We are still not able to simulate the ReRAM in the open-source analog flow, which is where we have been working. We also can not easily port over our designs with the proper PDK to Cadence, as there is no support for this at the moment. So, while this might not be helpful to our team now, this may be helpful for future teams that decide to work with ReRAM.

Finally, we came up with a solid work plan/division of labor for the rest of the work that needs to be done throughout the rest of the semester. We have hard deadlines on many things, as there is still quite a bit of work that needs to be done in a short amount of time. However, if we stick to this work plan, we believe that we will be able to satisfactorily meet the goals of this project.

Past Weeks Accomplishments

- Joshua Thater
    - Pushed Buffer, transmission gate, 2-1 MUX, and 4-1 MUX through the entire open-source analog design flow
    - Hooked up inverter in harness and other files to be run through precheck
    - Created layout of ReRAM cell and 1T1R cell that passed LVS
    - Updated final schematic once more
    - Created a detailed work plan for the rest of the semester
    - Added to documentation
        - This is almost done; finally
- Aiden Petersen
    - Passed pre-check on design
        - Found layout flaws causing issues and fixed them
        - Modified project files to fix pre-check “nitpicks”
    - Updated drivers to match the new model.
- Matt Ottersen
    - Finished pushing voltage dividers and 1-bit ADC through the analog design flow
- Regassa Dukele
    - Worked on designing the layout for individual components of ADC
    - Worked on the overall structure of the ADC

Pending Issues

- Verifying circuit design works as intended
- How to simulate our crossbar + compute design now that the crossbar will have to be “black boxed”

Individual Contributions

Team Member	Individual Contributions	BIweekly Hours	Total Hours
Joshua Thater	Pushed buffer, transmission gate, 2-1 MUX, 4-1 MUX, ReRAM cell, and 1T1R cell through the design flow.	28	139
Aiden Petersen	Pre-check and driver fixes.	15	95
Matt Ottersen	Finished ADC and voltage dividers	13	96
Regassa Dukele	Worked on the layout for individual components and op-amp	12	100

Plans for the Upcoming Weeks

- Joshua Thater
  - Create the layout of 8x8 crossbar + other crossbars for characterization
  - Finish up documentation + begin work on the analog side of the bring-up plan
  - Start hooking all of our components up in the harness layout
- Aiden Petersen
  - Document drivers and digital model setup
  - Create pretty schematics
  - Update drivers
  - Run pre-check on real design
- Matt Ottersen
  - Put all of the analog pieces components in one schematic and run simulations on them, including corner testing
- Regassa Dukele
  - Finishing up a layout for ADC and working on design verification
  - Component integration and running tests